

Design and Analysis of Single Phase Diode Clamped Multi Level Inverter

Dhanashri Kondbattunwar

Research scholar, Department of Electrical Engineering, Priyadarshini College of Engineering, Nagpur, India.

Sneha Wanjari

Assistant Prof. Chandan Kamble, Department Of Electrical Engineering, Priyadarshini College of Engineering, Nagpur, India.

Abstract – At present, multilevel inverters are extensively used in industries for high power and high voltage applications. Inverter can be broadly classified as two level inverter and multi level inverters. The multi level started with the three level converters. Minimum harmonic distortion is one of advantage of multilevel inverter. This paper deals with hardware design and analysis of three level diode clamped IGBT based inverter. The elementary concept of a multilevel converter is to achieve high power by using a series of a power semiconductor switches with lower voltage D.C source. The output voltage waveform of a multi-level inverter is comprises of the number of levels of voltages, typically obtained from capacitor voltage sources. In this paper, single phase diode clamp multilevel inverter topology is analyzed by employing SPWM technique which controls the switching operation with the help of Microcontroller programming and also the results are shown for the same.

Index Terms – Diode Clamp Multilevel Inverter, Sinusoidal PWM Technique.

1. INTRODUCTION

In recent years, industry has begun to demand higher power equipment. Multi-level inverters have been attracting increasing attention for power conversion in high-power applications due to their lower harmonics, higher efficiency, and lower voltage stress compared to two-level inverters. Multilevel inverter is a power electronics device which is capable of providing desired alternating voltage level at the output using multiple lower level D.C voltage as an input. Mostly a two level inverter is used in order to generate the A.C voltage from D.C voltage. Now the questions arises what is the need of using multilevel inverter when we have two-level inverter[2][4].

First we need to look at the concept of multilevel inverter. First take the case of a two level inverter. A two level inverter creates two different voltage for the load i.e suppose we are providing V_{dc} as an input to a two level inverter then it will provide $+V_{dc}/2$ and $-V_{dc}/2$ on output. To build up an AC output voltage these two voltages are usually switched with PWM. Though this method is effective it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a

problem but for some applications there may be a need for low distortion in the output voltage. The concept of Multilevel Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design become with more components and a more complicated controller for the inverter is needed.

2. DIODE CLAMP MULTILEVEL INVERTER TOPOLOGY

In this topology there are two pairs of switches and two diodes are consists in a three-level diode clamped inverter. All switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. The DC bus voltage is dividing into three voltage levels with the help of two series connections of DC capacitors, C_1 and C_2 . With the help of the clamping diodes D_{c1} and D_{c2} the voltage stress across each switching device is partial to V_{dc} . It is supposed that the total dc link voltage is V_{dc} and mid-point is synchronized at half of the dc link voltage, the voltage across each capacitor is $V_{dc}/2$ ($V_{c1}=V_{c2}=V_{dc}/2$). In a three level diode clamped inverter there are three different feasible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three-level inverter and so on.

3. WORKING

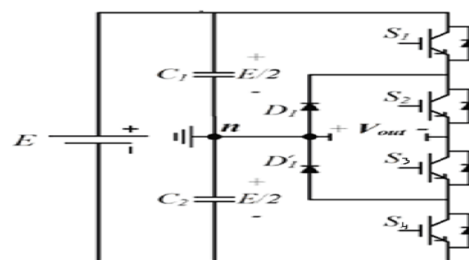


Fig 1: Circuit Diagram of three level inverter

Figure1 shows a three level diode clamp converter in which the dc bus consists of two capacitors C1 and C2. For dc-bus voltage E, the voltage across each capacitor is E/2 and each device voltage stress will be limited to one capacitor voltage level E/2 through clamping diodes.

Table1: Switching State Of The Three Level Diode Clamp Inverter

Switching status	State	Voltages
S1= ON,S2= ON	+ve voltage	$V_{ao}=V_{dc}/2$
S2=ON,S3=ON	0	$V_{ao}=0$
S3=ON,S4=ON	-ve voltage	$V_{ao}=-V_{dc}/2$

To explicate how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. Above table 1 shows that S1 and S3 are complementary each other. And similarly S2 and S4 are complementary each other.

4. CONTROL TECHNIQUES

The sinusoidal PWM technique is very popular for industrial converters. In this technique, an triangular carrier wave of frequency f_c is compared with the fundamental frequency f sinusoidal modulating wave and the points of intersection determines the switching points of power devices.

Three level pulse width modulated waveforms can be generated by sine-carrier PWM. Sine-carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves.

5. HARDWARE IMPLEMENTATION



Fig 2:-Hardware Model

A 230v AC supply is given to the primary of transformer and at the secondary side we are having five tapping. Across each tapping we get 0-15v. This 15v supply is given to the bridge rectifier which convert AC-DC. The 1000uf capacitor is used as a filter and to remove the ripple 0.1uf capacitor is used. Then the 7805 IC is connected to regulate the voltage. Then this 5v DC supply is given to the Microcontroller 89C52.

Across the another four tapping Driver IC is connected. This Driver IC requires 15v DC supply so the 15v DC supply is given through 7815 regulator IC. Microcontroller generate the pulses and this pulses are given to the Driver IC through NOT gate IC and a 100ohm resistor. Driver IC drive or control the switching of switches i.e IGBT through 1Kohm resistance and we are getting AC output voltage of 75-79V across “o” pole and middle of the leg.

To provide Dc supply to the IGBT leg. The arrangement is made with the help of (110-80-com-80-110) v transformer and rectifier filter circuit. The 230 AC supply is given to the primary of HV transformer and across secondary we getting 110v-com-110v supply. After this bridge rectifier (50-100v, 25 amp) is connected which converts the AC to DC. By using 470uf capacitor pulsating DC is converted into DC(pure) and also due to these capacitor the output voltage increases to 280-282v DC.

6. RESULTS

The pulses of the inverter is obtained over the oscilloscope to evaluate their amplitudes and frequencies.



Fig3:- Input Pulse

Output voltage waveform is found as follows

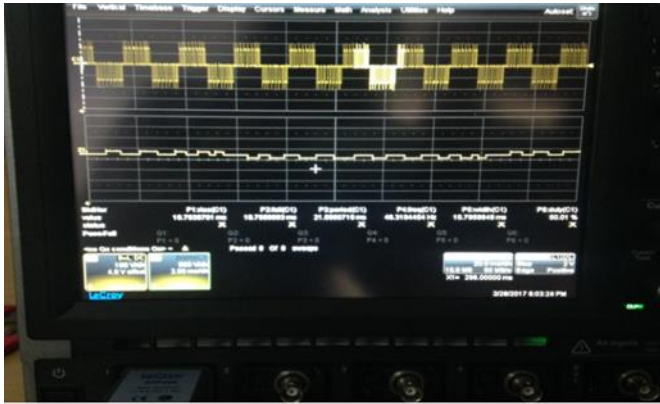


Fig 4:- Output Waveform

Output voltage in multi meter is found as 75v.

7. CONCLUSION

The hardware of single phase 3-Level Diode clamped multilevel inverter was carried using sinusoidal pulse width modulation (PWM) and analyzed the performance of THD and FFT analysis three level diode clamped multilevel

inverter and their output waveforms.

REFERENCES

- [1] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng, senior member, IEEE “multilevel inverters: a survey of topologies, controls, and applications” IEEE transactions on industrial electronics, vol. 49, no. 4, august 2002
- [2] Charles I. Odeh and Marcel U. Agu “new topology for single-phase, three-level, SPWM VSI with LC filter “, department of electrical engineering, university of nigeria, nsukka.
- [3] Muhammad H. Rashid, “power electronics, circuits, devices, and applications”, third edition, pearson education, inc.,2004
- [4] Andreas Nordvall, “Multilevel Inverter Topology Survey”, Master of Science Thesis in Electric Power Engineering, Department of Energy and Environment, Division of Electric Power Engineering, CHALMERS UNIVERSITY OF TECHNOLOGY, Goteborg, Sweden, 2011.
- [5] E. Beser, S. Camur, B. Arifoglu, E. Kandemir Beser, “A grid connected photovoltaic power conversion system with single phase multilevel inverter,” Solar (2010), pp. 2056-2067.
- [6] Jagdish Kumar, Biswarup Das and Pramod Agarwal, “Harmonic Reduction Technique for a Cascade Multilevel Inverter”, International Journal of Recent Trends in Engineering, Vol 1, No. 3, May 2009.
- [7] E. Kandemir Beser, B. Arifoglu, S. Camur and E Beser “Design and Application of a Single Phase Multilevel Inverter Suitable for using as a Voltage Harmonic Source”, Journal of Power Electronics, Vol. 10, No.2, March 2010.